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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,556	08/17/2001	Gerard Chauvel	TI-32850	3902

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EXAMINER	
TRUONG, LECHI	
ART UNIT	**PAPER NUMBER**
2194	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,556	CHAUVEL, GERARD	
	Examiner	Art Unit	
	LeChi Truong	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/29/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 are presented for the examination.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 8 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 8 of US Patent number: 7,120,715 (the application number 09/932866). Although the conflicting claims are not identical, they are not patentably distinct from each other because both computer systems comprise substantially the same elements. Both the application and the patent teach priority access to shared resource in a digital system having a plurality of devices, associating priority values to the requests, arbitrating for accessing shared resource by using the priority associated with the request, a plurality of memory management units stores a plurality of page entries and has output priority vale, the arbitration circuitry connected to receive a request signal from each of the plurality of devices and the associated access priority value from each MMU, arbitration circuitry is operable to

schedule access to the shared resource according to the access priority value and the address space priority value.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1-5, 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe et al (US. 5,906,000) in view of Barnaby et al (US. Patent 6,006,303).

As to claim 1, Abe teaches the invention substantially as claimed including: access to the shared resource (col 3, ln 52-55), address space regions (the address 44 of the caches memory 18, col 4, ln 17-21/ Fig. 2), an address space of the shard resource (the cache memory 18, col 3, ln 65-67), organizing an address space of the shared resources into address space regions (col 1, ln 56-59 / col 4, ln 20-23), access priority value (a priority corresponding to each data, col 1, ln 56-58), assigning individual access priority value to a plurality of the address space regions(col 1, ln 55-59/ col 4, ln 19-23), initiating an access request (col 1, ln 59-63/ col 38-41), the access request specifies a target address within the address space of the shared resource(col 5, ln 22-26/ col 6, ln 12-19), providing an access priority value with the access request(a priority to be assigned to the read data, col 5, ln 21-24/ col 7, ln 13-16), the access priority value corresponds

to an access priority value assigned to an address space region selected by the target address(compares a priority stored in the tag of the one cache block, with the priority of the new data to be written(the priority obtained from the priority table 16)/ at the time, a tag corresponding to the cache block with the new data stores a priority corresponding to the new data and obtained from the priority table, col 5, ln 44-46/ ln 67 to col 6, ln 1-3/ln 17-21/col 7, ln 17-21), access to the shared resource by using the access priority value(col 1, ln 60-67/ col 7, ln17-21).

Abe does not explicitly teach a plurality of devices for access to shared resources, arbitrating between multiple pending requests to the share resource based on the access priority value assigned to each pending request. However, Barnaby teaches a plurality of devices for access to a shared resources (a shared resource access system controls access by a plurality of devices to a shared resource, col 12, ln 17-20), arbitrating between multiple pending requests to the share resource based on the access priority value assigned to each pending request (compares priority values of pending resource access requests and determines a winning request… an arbiter which arbitrates between a currently active resource access request and a winning request form the priority decoder, col 12, ln 19-27).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Abe and Barnaby because Barnaby's a plurality of devices for access to a shared resources, arbitrating between multiple pending requests to the share resource based on the access priority value assigned to each pending request, would improve the flexibility of Abe's system by allowing the clients always request access when it has data, and be granted access based on how much latency it has experienced while requesting the access.

As to claim 2, Abe teaches an access priority value to an address space region according to a program or data stored within the address space region (col 2, ln 36-37).

As to claim 3, Abe teaches assigning a first access priority value to a first one of the several address space regions and assigns a different access priority value to a second one of the several address space regions (col 1, ln 56-58).

As to claim 4, Abe teaches a plurality of program tasks occupy a single address space regions (col 3, ln 47-50).

As to claim 5, Abe teaches starting a program task (col 4, ln 39-42), determining an access priority value specified by the program task (col 4, ln 40-41), allocating an address space region for the program task (col 6, ln 12-17/ col 6, ln 46-50), assigning the access priority value specified by the program task to the address space region allocated for the program task (col 6, ln 12-17/ col 6, ln 46-50).

As to claim 7, Abe teaches an execution priority value of a program task to which the address space region is allocated (col 7, ln 19-21).

5. Claims **8, 9 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayanan et al (US. Patent 4,814,974) in view Odenheimer (US. Patent 4,818,932) and further in view of Welland (US. Patent 5,581,722).

As to claim 8, Narayanan teaches a digital system (digital control, col 1, ln 21-22), a shared resource (a resource, col 2, ln 47-48/ ln 63-64), a plurality of devices (devices, col 1, ln 21-22/ ln 63-64), a plurality of devices connected to access the shared resource (col 1, ln 21-22),

a memory unit (memory unit, col 7, ln 20-21), a plurality of page entries and each page entry has an access priority field (col 2, ln 49-55/ col 7, ln 52-59), output an access priority value in response to received a request(col 5, ln 30-34/col 4, ln 26-30), arbitration circuitry connected to receive a request signal from each of the plurality of device and an access priority value from each memory unit(The network 67 reorders the request lines 31-46 in order of the priority of their associated devices 0-15, as specified by the inputs from the priority generators 71-86, col 5, ln 9-13, connect the generators 71-86 to control ports of a permutation network 67, col 4, ln 67 to col 5, ln 1-2/ the request lines 31-46 from the devices 0-15 respectively are connected to an input port of the permutation network 67, col 5, ln 4-7/ col 4, ln 26-29/ ln 51- 55/ abstract ln 5-11 and ln 21-26)/ the arbitration circuitry is a permutation network 67 of arbitrator 27, a request signal is a request lines 31-46, the access priority is a the inputs from the priority generators 71-86,(col 4, ln 52-60/ Fig. 2), the arbitration circuitry is operable to schedule access to the shared resource according to the access priority values(col 4, ln 26-30).

Narayana do not explicitly teach a memory unit as MMU and receiving an address and output an access priority associated with a received address. However, Odenheimer teaches a memory unit as MMU (the MMU includes a set of three interface port and a pair of DRAM controllers, col 7, ln 55-59), and receiving an address (the address provided by the microprocessor whether the data is to stored in the event or in the odd bank and transmits appropriate single bit EREQ (two bit odd request single) and OREQ (two bit even signal) signals to the event or odd DRAM controllers indicating which memory bank is to received data, col 8, ln 15-20), and output an access priority associated with a received address(The DRAM controller contain arbitration with monitor the OREQ and EREQ signals/ the DRAM controller

for the bank checks the states of all the request signals and honor request in order priority, col 9, ln 4-8/ ln 27-33/ the arbitrator of DRAM controller give bit OREQ signal from the microprocessor interface port next highest priority, col 15, ln 52-54).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Abe and Odenheimer because Odenheimer's a memory unit as MMU and receiving an address and output an access priority associated with a received address would improve the flexibility of Abe's system by reducing competition for access to a random access memory by a plurality of data processing devices.

Narayanan and Odenheimer do not teach plurality of MMUs. However, Welland teaches plurality of MMUs (Memory Management units, col 1, ln 50-51)

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Narayanan, Odenheimer and Welland because Welland's a memory unit as MMUs would improve the efficiency of Narayanan and Odenheimer's systems by allowing plurality of memory management units (MMUs) to control a CPU's right access a memory in order to initiate performance of operation.

As to claim 9, Welland teaches a translation lookaside buffer (TLB (translation lookaside buffer), col 2, ln 47-48).

As to claim 11, Narayanan teaches the shared resource is a bus, a plurality of memory-mapped resources connected to the bus (col 4, ln 26-30).

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Narayanan et al (US. Patent 4,814,974), Odenheimer (US. Patent 4,818,932) in view of Welland (US. Patent

5,581,722), as applied to claim 8 above, and further in view of David Eck(xLogicCircuits Lab 2: Memory Circuits).

As to claim 10, Narayanan, Odenheimer and Welland do not teach a memory circuit. However, David teaches memory circuit (memory circuit, page 5, section Random Access Memory, ln 1).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Narayanan, Odenheimer, Welland and David because David 's memory circuit would increase the efficiency of Narayanan, Odenheimer, Welland's systems by holding several different binary numbers, which can be used to represent both program and data.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Narayanan et al (US. Patent 4,814,974), Odenheimer (US. Patent 4,818,932) in view of Welland (US. Patent 5,581,722), as applied to claim 8 above, and further in view Lysejko et al (US. Patent 5,918,160).

As to claim 12, Narayanan, Odenheimer and Welland do not teach a wireless communication, a display, radio frequency circuitry, and an aerial. However, Lysejko teaches a wireless communication, a display, radio frequency circuitry (Wireless telecommunications system, col 3, ln 61-62/ display 810, col 15, ln 30-31/ radio frequency circuitry, col 10, ln 55-56/ an aerial, col 25, ln 12-13).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Narayanan, Odenheimer, Welland and Lysejko because Lysejko's a wireless communication, a display, radio frequency circuitry would improve the efficiency of Narayanan, Odenheimer, Welland's systems by providing a subscriber station of a wireless telecommunications system which comprises transmitter/receiver for wireless communication.

Allowable Subject Matter

7. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LeChi Truong whose telephone number is (571) 272 3767. The examiner can normally be reached on 8 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

LeChi Truong

September 27, 2006

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER